Capacitive Inter-Chip Data and Power Transfer for 3-D VLSI

Eugenio Culurciello, *Member, IEEE*, and Andreas G. Andreou, *Member, IEEE*

***Abstract*—We report on inter-chip bidirectional communication and power transfer between two stacked chips. The experimental prototype system components were fabricated in a 0.5-μm silicon-on-sapphire CMOS technology. Bi-directional communication between the two chips is experimentally measured at 1 Hz–15 MHz. The circuits on the floating top chip are powered with capacitively coupled energy using a charge pump. This is the first demonstration of simultaneous nongalvanic power and data transfer between chips in a stack. The potential use in 3-D VLSI is aimed at reducing costs and complexity that are associated with galvanic inter-chip vias in 3-D integration.**

***Index Terms*—AC coupling, capacitive coupling, chip-to-chip communication, multichip module, proximity communication, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), three-dimensional (3-D) integration.**

I. Introduction

THREE-DIMENSIONAL (3-D) integrated circuits are emerging as a viable technology for information processing in high throughput sensor arrays [1]–[4] and massively parallel computer architectures that benefit from locality of reference and short interconnects in the third dimension [5]–[7].

The early attempts towards 3-D integration were focused on multiple tiers with polycrystallized silicon devices [8]. An alternative approach that has emerged in the recent years uses wafers fabricated in standard CMOS technologies, augmented with an inter-die via [9]. The bulk CMOS wafers are first thinned down to about 10-μm thickness and then aligned and bonded to form a multiwafer stack. The whole process poses significant challenges with bulk CMOS material, and recently an alternative approach has been demonstrated using silicon-on-insulator (SOI) CMOS wafers [3]. This has lead to the first multiproject foundry 3-D run at the MIT Lincoln Laboratories [4]. Even with SOI CMOS wafers the whole process is prohibitively expensive for mass production and fabrication yields are low. The advantages of 3-D architecture can also be achieved using virtual *vias* for through wafer communication. Virtual optical *vias* [9], [10] as as well as inductive *vias* [11] have been reported for 3-D interconnects. Virtual optical and inductive vias simplify the integration process, as they do not require galvanic connections, but they do not compete with the interconnect density of metal vias of modern CMOS fabrication processes and 3-D processes [4]. Capacitive vias offers another potential method for inter-chip communication. Capacitive inter-die coupling has been used successfully only to transfer signals [12]–[14], between dies, circuit boards [15] and multichip modules, while still requiring electrical connections for both dies in order to provide the required power supply [16]. These physical connection are generally obtained using a ball grid array, wire bonds or probes, all imposing mechanical and cost limitations on the number and density of data signal connections to the package.

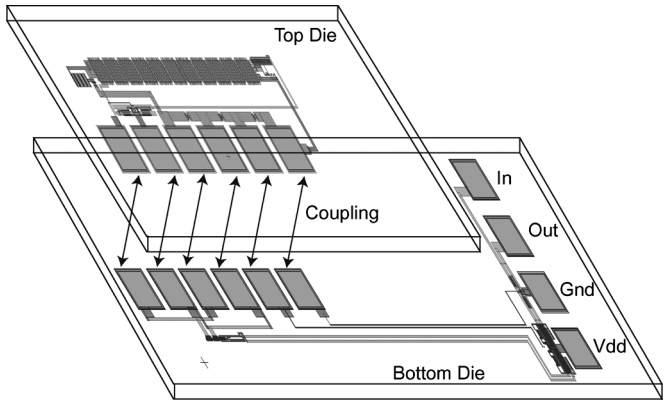

Fig. 1. Three-dimensional prototype for bidirectional communication between two dies. The bottom die is connected galvanically through bonding pads to external power supply and signals. The top die features capacitive inter-chip data and power transfer with no galvanic connections.

In this brief, we report on the first multichip module that uses nongalvanic capacitive coupling to provide both bi-directional communication and also transfer of power between two separate dies. A prototype was assembled using components that were fabricated on a commercially available 0.5-μm silicon-on-sapphire (SOS) process. The proposed 3-D integration technique does not necessitate any specialized fabrication technique or equipment. In addition, the alignment of the dies is simplified by the transparency of the sapphire substrate of SOS dies.

II. System Overview

The prototype consists of two SOS CMOS dies, one acting as transmitter and one as receiver. The transmitter die (*bottom* die) is placed and bonded into a common dual-in-line package. The receiver die (*top* die) is flipped and aligned on top of the transmitter die, so that the required capacitive coupling is formed between metal pads on both dies. Fig. 1 shows the alignments of the pads between the transmitter bottom circuit and the receiver circuit. In this demonstration the alignment of the dies was performed manually under an optical microscope and hence

Manuscript received October 18, 2005. This work was supported by the Johns Hopkins Applied Physics Laboratory, MD, by NASA Mars Advanced Technology Development under Grant 1243213, and by the National Science Foundation under Grant NSF-ECS-0225489 and Grant NSF-ECS-GOALI-0010026. This paper was recommended by Associate Editor R. Puri.

E. Culurciello is with the Department of Electrical Engineering at Yale University, New Haven, CT 06520 USA (e-mail: eugenio.culurciello@yale.edu).

A. G. Andreou is with the Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD 21218 USA (e-mail: andreou@jhu.edu).

Digital Object Identifier 10.1109/TCSII.2006.885073

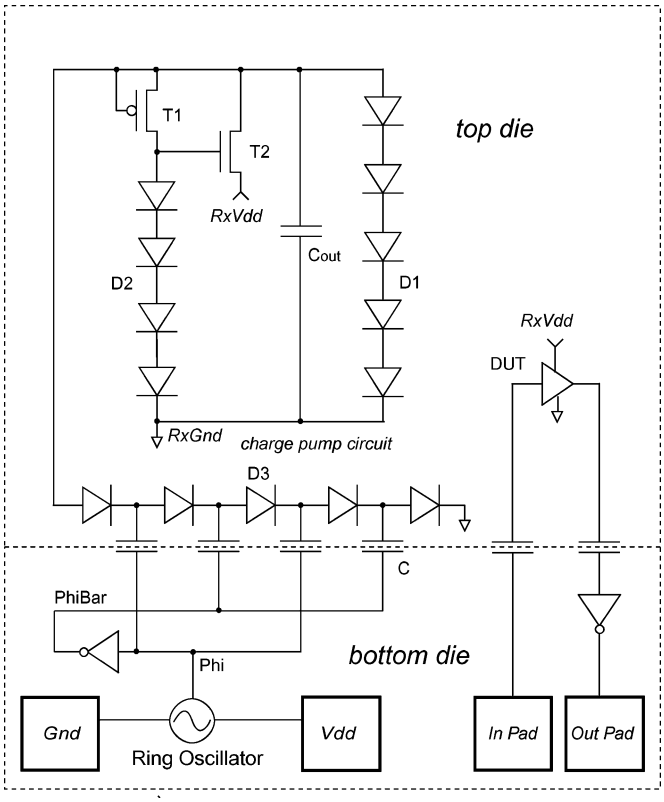

Fig. 2. System architecture: a distributed charge pump is used to transfer the power using capacitive coupling between two dies. The DUT, powered by the charge pump, receives and communicates a signal to the bottom die.

the precision of the alignment was 15 μm. The alignment under optical light is possible thanks to the transparency of the SOS substrate. The dies have been bonded together using a layer of transparent varnish. Submicrometer precision can be obtained in the alignment when using a dedicated aligner bonder machine. Six metal pads are aligned in this demonstration, four of which are used by a charge-pump circuit and two more for bidirectional communication of two signals. The charge pump is used to exchange power between dies. The circuits in Fig. 1 are actual layout of the fabricated circuit, while Fig. 5 (shown later) is a micrograph of the multi chip module. The coupling metal plate capacitance is 8 fF, with a plates distance of 10 μm ($3 + 3$ μm for the bond to passivation step and an estimated 4 μm for the varnish layer). These distances can be reduced using a simple blanket reactive ion etching of the glass passivation layer.

Fig. 2 shows a schematic of the prototyped system with implementation details of the transmitter and receiver circuits. The bi-directional communication circuit (right side of Fig. 2) is composed of an input pad (*in*) at the receiver circuit which is bonded to the package for external stimulation. The input pad is connected capacitively to the receiver circuit which uses a digital buffer [device under test (DUT)] to relay the digital signal and drive the return coupling capacitance. The signal is buffered again and output to a pad of the transmitter circuit (OUT). Coupling of power is performed by the charge-pump circuit on the left side of Fig. 2. The pump circuit is split between the top and bottom dies. The bottom dies contains the galvanic connections to the power supply pads V_{dd} and Gnd. The DUT is composed of four digital inverters and is powered from the charge-pump output.

III. Charge-Pump Circuit

The charge-pump circuit is used to transfer power from the bonded bottom die to the floating top die. Fig. 2 shows the architecture of the N-stages Dickson [17], [18] charge pump. The circuit uses two square wave pumping clocks ϕ, and $\bar{\phi}$ (Phi and $PhiBar$ in Fig. 2) to pump charge through coupling capacitors C. The output voltage R_xV_{dd} of the Dickson charge pump is given by

$$R_xV_{dd} = V_{\text{in}} + N\left(\frac{C}{C+C_S}V_\phi - V_D - \frac{I_{\text{out}}}{(C+C_S)f_\phi}\right) - V_D. \tag{1}$$

C_S is the ground parasitic capacitance of each capacitor C (not shown in the figure). V_ϕ is the voltage amplitude of the clock ϕ and f_ϕ is the clock frequency. With ideal diodes and capacitors, each stage increments the voltage R_xV_{dd} by a step equal to V_ϕ. The diode is employed in each stage to constrain the charge flow in one direction allowing capacitors C to charge, but not to discharge. The built-in diode voltage drop reduces the pumping voltage, subtracting V_D from the voltage pumped at each stage. The open circuit output voltage of the charge pump is reduced by the load current I_{out} [last term in parenthesis of (1)].

An eleven-stage ring oscillator produces a 350-MHz square-wave clock signal to drive the pump, and it is represented by an oscillator symbol in Fig. 2. The output of the oscillator is buffered to drive the pumping capacitances C. These capacitors are designed using a parallel plate configuration of bonding pads. Facing bonding pads of the top and bottom dies create two parallel plates. Each capacitance has a value that depends on the distance between the bonding pads plates (here approximately 8 fF).

To optimize the design of the Dickson charge-pump circuit, we employ MOS transistors with different threshold voltages that are available in the Peregrine SOS CMOS process [10], [19]. The following naming convention is employed to identify the device: regular Rx threshold ($V_{\text{TH}} \approx 0.7$ V), low xL threshold transistors ($V_{\text{TH}} \approx 0.3$ V, and intrinsic Ix, zero threshold transistors ($V_{\text{TH}} \approx 0$ V). The type of transistor is denoted by substituting x for either N or P. Diodes D1 are diode connected regular threshold transistors that are employed by the technology vendor as ESD protection diodes.

Diode connected NL MOS transistors are used as the rectifiers (D3) in each pump stage. The use of a low-threshold MOS transistor in this part of the circuit minimizes the forward bias diode drop V_D to 0.3 V, and reduces the undesirable voltage drops on the rectifiers. A 9-pF capacitor at the output (C_{out}) together with a series of five diodes (D1) are used as the charge-pump filter and constraint the maximum voltage within the maximum supply range of the process (3.3 V). Transistors T1, T2, and a diode chain of four diodes D2 form an active voltage regulator at the output of the charge pump to produce the regulated voltage R_xV_{dd}. The series regulator transistor T2

TABLE I
DEVICE TYPE AND SIZE OF MOS TRANSISTORS USED IN THE CHARGE-PUMP CIRCUIT

Device	Type	Size [μm]
D1	RN	27.4/1.6
D2	RN	2/2
D3	NL	15/0.5
T1	IP	10/2
T2	IN	6/4

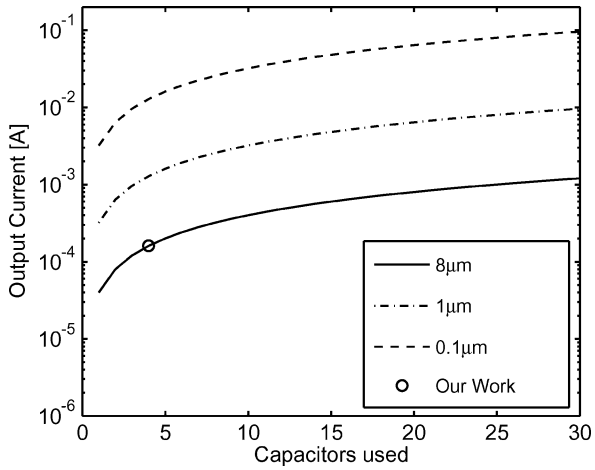

Fig. 3. Scaling properties of the charge pump in relation to the distance between the plates of coupling capacitors. Decreasing the distance between the plates increases the capacitance and the coupled energy. The capacitor plates were $90 \times 90\ \mu\text{m}^2$.

is a zero threshold IN device biased by a string of four regular threshold (RN) diode connected MOS transistors (D2) and a current source. Transistor T1 is a self-biased current source implemented using an IP MOS transistor. Transistor T2 acts as an ideal voltage follower without a build-in voltage. The device type and sizes are given in Table I.

The absence of substrate parasitics in the SOS CMOS process eliminates all the stray capacitance to ground C_S that further degrade the voltage gain of each stage (see (1)). The stray capacitance in a 0.5-μm bulk-process can have a value of up to 10% of the nominal value (from extracted parameters [20]). For example a capacitance of $C = 450$ fF can have a parasitic $C_S = 45$ fF. The capacitance C obtained with the SOS process has virtually zero parasitic capacitance, thus the ratio $C/(C+C_S)$ is 1 in SOS CMOS and 0.9 in a bulk CMOS. For a design with no parasitic capacitances, such as the one presented in this brief, (1) simplifies to

$$V_{\text{out}} = V_{\text{in}} + N\left(V_\phi - 0.3 - \frac{I_{\text{out}}}{Cf_\phi}\right) - 0.3. \qquad (2)$$

Solving (2) results in a value of the unloaded V_{out} of 11.7 V, with a supply of 3.3 V, $V_{\text{in}} = 0$ V, $V_D = 0.3$ V, $N = 4$, $I_{\text{out}} = 0$ A. The equivalent result in a bulk process of (1) is V_{out} of 8.3 V with a $V_D = 0.7$ V.

Fig. 3 plots the scaling properties for the charge-pump output current as a function of capacitors (pumping stages) and the distance between capacitors' plates. The current was calculated using the terms between parenthesis in (2). We used the above design parameters, and $90 \times 90\ \mu\text{m}^2$ bonding pad plates separated by silicon dioxide. The charge-pump output current is calculated for an unloaded and unprotected pump. The charge pump used in this article provided approximately 100 μA of current, as can be seen in Fig. 3. Some of this current is used in the series active voltage regulator. Decreasing the distance between the capacitor plates increase the coupling capacitance. By thinning the passivation layer between the two dies, shorter plate distances can be obtained. The charge-pump output current can be increased to several milliamperes by using capacitors with 1-0.1-μm plates distance and SiO_2 dielectric.

IV. RESULTS

We successfully tested the functionality of the communication link and power transfer at signal frequencies ranging from 1 Hz to 15 MHz. The results extend to 100 MHz reliably in simulations, assuming tighter coupling (not achieved in this experimental prototype). Fig. 4 shows screen shot from the oscilloscope during measurements. For each screen the top waveform is the input signal at the transmitter and the bottom waveform is the output signal from the receiver. The top left is at 1-V supply and 1-MHz input. The top right is at 3.3 V and 1 kHz, the bottom left at 1 MHz and the bottom right at 15-MHz input frequency. The current drawn was 9 mA at 3.3-V supply from 1 kHz to 15 MHz.

V. DISCUSSION AND TECHNOLOGY COMPARISON

Capacitive coupling of data and power of SOS circuits is a cost-effective solution for 3-D assemblies of two facing dies or flip-chip packaging of single dies on a printed circuit board. The high packaging cost of galvanic connections as bonding wires is virtually eliminated when standard bonding pads are used as coupling capacitors. In addition, small coupling pads can be used and circuits can be designed under the coupling pads, as opposed to standard bonding pads, where the mechanical stress of the bonding equipment would damage underlying circuits.

The capacitive vias used in our prototype occupy an area of $90 \times 90\ \mu\text{m}^2$ for a plate separation of 10 μm. By keeping the coupling capacitance constant, this area can be reduced to $30 \times 30\ \mu\text{m}^2$ with a plate separation of 1 μm, and to $9 \times 9\ \mu\text{m}^2$ with a 0.1 μm separation. Typical inductive vias occupy an area between $100 \times 100\ \mu\text{m}^2$ [11] and $300 \times 300\ \mu\text{m}^2$ [21]. Inductive vias of $50 \times 50\ \mu\text{m}^2$ have been proposed, but no demonstration of communication was given [12]. Three-dimensional galvanic vias occupy an area of $5 \times 5\ \mu\text{m}^2$ in the DARPA-sponsored 3-D SOI process from MIT Lincoln Laboratories [22]. Fig. 5 is a micrograph of the multi chip module. The size of the vias are compared in Fig. 6. Through-die galvanic vias obtained in 3-D processes obtain very high density of vertical connections, but require expensive fabrication technologies. Capacitive coupling requires less silicon area than inductive coupling, especially when plates are close to each other. Plate spacing of 1 μm or less can be obtained easily by etching the passivation layer of facing dies.

Capacitive vias can be optimized for power and signal transfer. When transferring data, low capacitance vias are

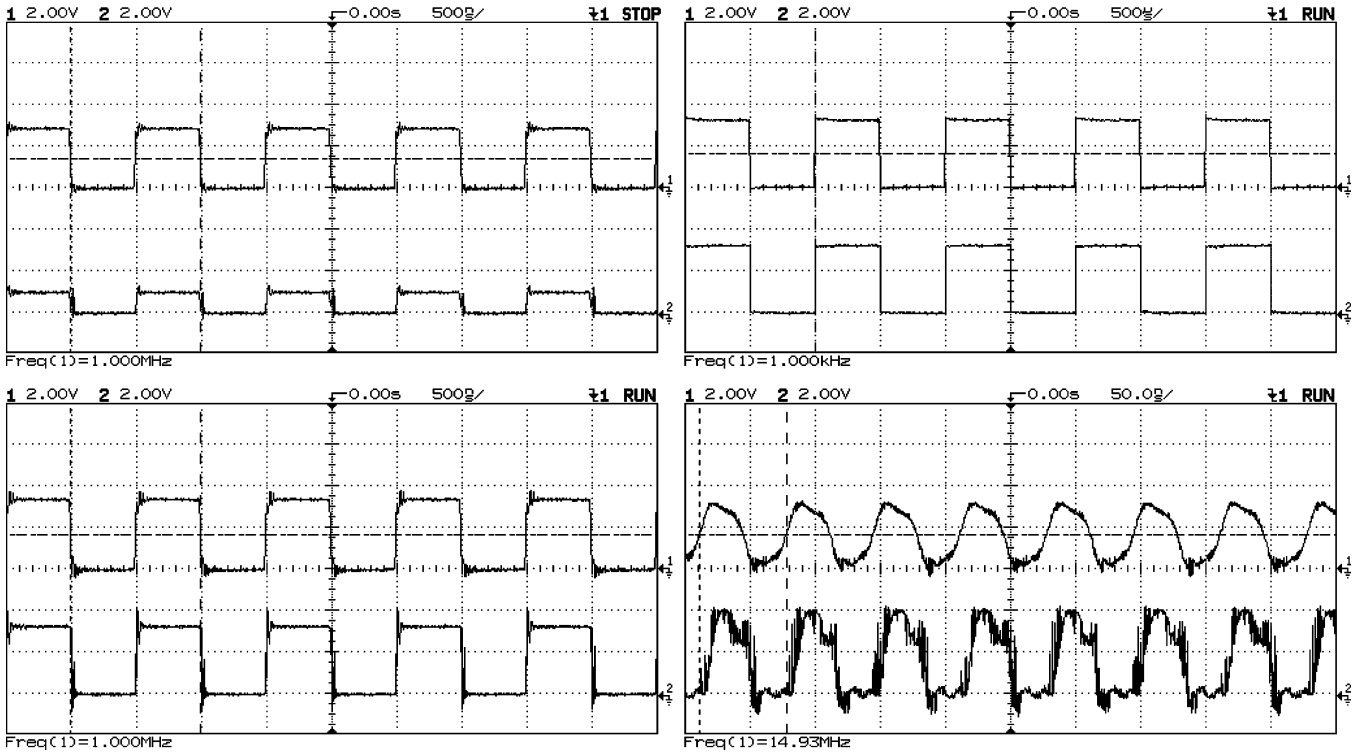

Fig. 4. Oscilloscope traces verifying functionality of the prototype system.

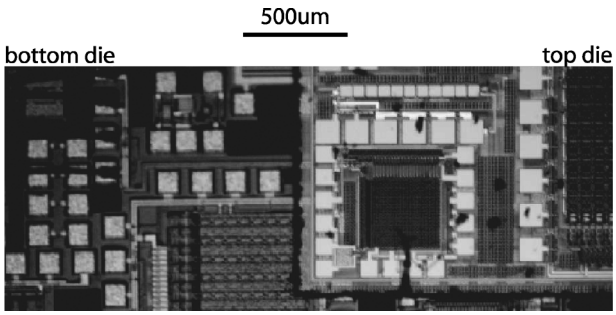

Fig. 5. Micrograph of the assembled multi chip module.

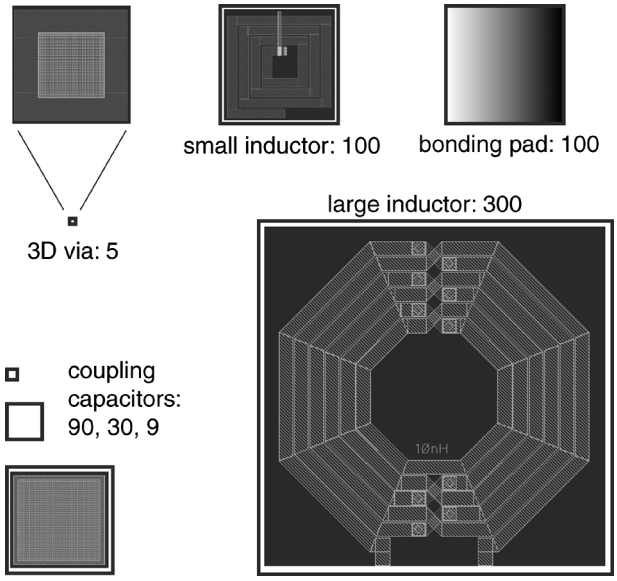

Fig. 6. Comparison between layout sizes of inductive, capacitive and galvanic vias for data communication. The large inductor (10 nH) and the 3-D via is in the MIT LL 3D-SOI process. A magnified ($20\times$) 3-D via layout is also displayed. The capacitive vias and the small inductor (1 nH) are SOS layouts. The solid square is the size of a bonding pad, here reported as a frame of reference. Sizes are in (linear) micron.

desirable because less power consumption is required to drive them. On the other hand, the capacitive vias used to couple power should be obtained with large coupling capacitances, so that power transfer is maximized. This in turn requires more silicon area. The required silicon area for a given power can be obtained from Fig. 3.

It is important to notice that capacitive coupling provides electrical insulation between dies [18], [23]. This feature is advantageous for the design of sensitive instruments that needs to be decoupled from noise sources. In addition, insulation is often required in body-implants and biomedical circuits for the safety of patients and users.

In summary, capacitive coupling of data has been demonstrated practical and advantageous in 3-D assemblies and die packaging. Capacitive coupling of power is particularly suitable for low-power sensors and sensory front-ends. Insulated sensory systems running on low power budgets can also take advantage of the technology to decouple circuitry.

ACKNOWLEDGMENT

The fabrication was provided by MOSIS.

REFERENCES

[1] H. Kurino, K. W. Lee, T. Nakamura, K. Sakuma, N. Miyakawa, H. Shimazutsu, K. Kim, and M. Koyanagi, "Intelligent image sensor chip with three dimensions structure," in *Proc. IEEE Int. Electron. Devices Meetingg*, 1999, pp. 879–882.

[2] M. Koyanagy, Y. Nakagawa, K. W. Lee, T. Nakamura, Y. Yamada, K. Park, and H. Kurino, "Neuromorphic vision chip fabricated using three-dimensional integration technology," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2001, vol. 1, pp. 270–271.

[3] J. Burns, L. McIlrath, J. Hopwood, C. Keast, D. Vu, K. Warner, and P. Wyatt, "An SOI three-dimensional integrated circuit technology," in *Proc. IEEE Int. SOI Conf.*, Oct. 2000, pp. 20–21.

[4] V. Suntharalingam, R. Berger, J. Burns, C. Chen, C. Keast, J. Knecht, R. Lambert, K. Newcomb, D. O'Mara, C. Stevenson, B. Tyrrell, K. Warner, B. Wheeler, D. Yost, and D. Young, "CMOS image sensor fabricated in three-dimensional integrated circuit technology," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, vol. 1, pp. 356–357.

[5] K. W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, H. Hashimoto, K. T. Park, H. Kurino, and M. Koyanagi, "Three-dimensional shared memory fabricated using wafer stacking technology," in *Proc. IEEE Int. Electron. Devices Meetingg*, 2000, pp. 165–168.

[6] X. Lei, C. C. Liu, H. S. Kim, S. K. Kim, and S. Tiwari, "Three-dimensional integration: technology, use, and issues for mixed-signal applications," *IEEE Trans. Electron Devices*, vol. 50, pp. 601–609, Mar. 2003.

[7] A. Topol, D. LaTulipe, and L. Shi *et al.*, "Enabling SOI-based assembly technology for three-dimensional (3d) integrated circuits (ICs)," in *Proc. IEEE Electron Devices Meeting*, Dec. 2005, pp. 352–355.

[8] R. Buchner, W. VanDerWel, K. Haberger, S. Seitz, J. Weber, and P. Seegebrecht, "Process technology for 3D-CMOS devices," in *Proc. IEEE SOS/SOI Technol. Conf.*, Oct. 1989, pp. 72–73.

[9] M. Koyanagi, H. Kurino, K. W. Lee, K. Sakuma, N. Miyakawa, and H. Hitano, "Future system-on-silicon LSI chips," *IEEE Micro*, pp. 18–22, Jul.–Aug. 1998.

[10] A. G. Andreou, Z. K. Kalayjian, A. Apsel, P. Pouliquen, R. A. Athale, G. Simonis, and R. Reedy, "Silicon-on-sapphire CMOS for optoelectronic microsystems," *IEEE Circuits Syst. Magazine*, vol. 1, no. 3, pp. 22–30, 2001.

[11] D. Mizoguchi, Y. B. Yusof, N. Miura, T. Sakura, and T. Kuroda, "A 1.2 Gb/s/pin wireless superconnect based on inductive inter-chip signaling (IIS)," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2004, vol. 1, pp. 142–144.

[12] S. E. Mick, J. M. Wilson, and P. Franzon, "4 Gbps AC coupled interconnection," in *Proc. IEEE Custom Integr. Conf.*, May 2002, pp. 133–140.

[13] K. Kanda, D. Antono, K. Ishida, H. Kawaguichi, T. Kuroda, and T. Sakurai, "1.27 Gb/s/ch 3 mW/pin wireless super connect (WSC) interface scheme," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 2003, vol. 39, pp. 186–187.

[14] R. Drost, R. Hopkins, R. Ho, and I. Sutherland, "Proximity communication," *IEEE J.Solid-State Circuits*, vol. 39, no. 9, pp. 1529–1535, Sep. 2004.

[15] J. Kim, J. Choi, C. Kim, A. Chang, and I. Verbauwhede, "A low power capacitive coupled bus interface based on pulsed signaling," in *Proc. IEEE Custom Integr. Conf.*, Oct. 2004, vol. 1, pp. 35–38.

[16] S. E. Mick, L. Luo, J. M. Wilson, and P. Franzon, "Buried bump and AC coupled interconnection technology," *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 121–125, Feb. 2004.

[17] J. Dickson, "On-chip high-voltage generation in nMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. SC-6, pp. 374–378, Jun. 1976.

[18] E. Culurciello, P. Pouliquen, and A. Andreou, "An isolation charge pump fabricated in silicon-on-sapphire CMOS technology," *Electron. Lett.*, vol. 41, no. 10, pp. 590–592, May 2005.

[19] Peregrine, 2005 [Online]. Available: http://www.psemi.com/

[20] MOSIS, 2005 [Online]. Available: http://www.mosis.org

[21] K. Chong and Y. Xie, "High-performance on-chip transformers," *IEEE Electron Device Lett.*, vol. 26, pp. 557–559, Aug. 2005.

[22] MITLL, Low-power FDSOI CMOS process application notes MIT Lincoln Laboratories, Cambridge, MA, Dec. 2004.

[23] E. Culurciello, P. Pouliquen, A. Andreou, K. Strohbehn, and S. Jaskulek, "A monolithic digital galvanic isolation buffer fabricated in silicon-on-sapphire CMOS," *Electron. Lett.*, vol. 41, no. 9, pp. 526–528, Apr. 2005.